AN10001
S5KM312CL Hardware Design Guide

Application Note Rev.1.2

Introduction

This document is an extension of the hardware design section of the S5KM312CL Data Sheet for mmWave sensor chips. It provides detailed information on schematic design and PCB layout considerations to help users become familiar with and use the chip more efficiently, ensuring accurate completion of schematic design and PCB layout tasks.

This document is primarily intended for the following users:

- Hardware design engineers;
- Technical support engineers.

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1 Power Supply Configuration

The S5KM312CL chip offers two power supply options:

- Single power supply at 3.3 V;
- Dual power supply at 3.3 V and 1.6 V.

When selecting a power supply scheme, it is essential to consider the following:

- When using a single 3.3 V power supply, the 1.6 V voltage output from the chip's internal DCDC is intended solely for the chip's use. It is not recommended for powering external components.
- When using dual power supplies, it is crucial to select external DCDC/LDO chips carefully, especially in long- range application scenarios, to ensure that the internal DCDC's switching frequency does not interfere with the intermediate-frequency signals.

1.1 Single Power Supply

When the chip is powered by a single 3.3 V supply, the internal DCDC provides 1.6 V to the chip. Pin 16 (DCDC_SW) of the chip connects to a 22 μH inductor, and a parallel 22 μF capacitor, as shown in Figure 1-1.

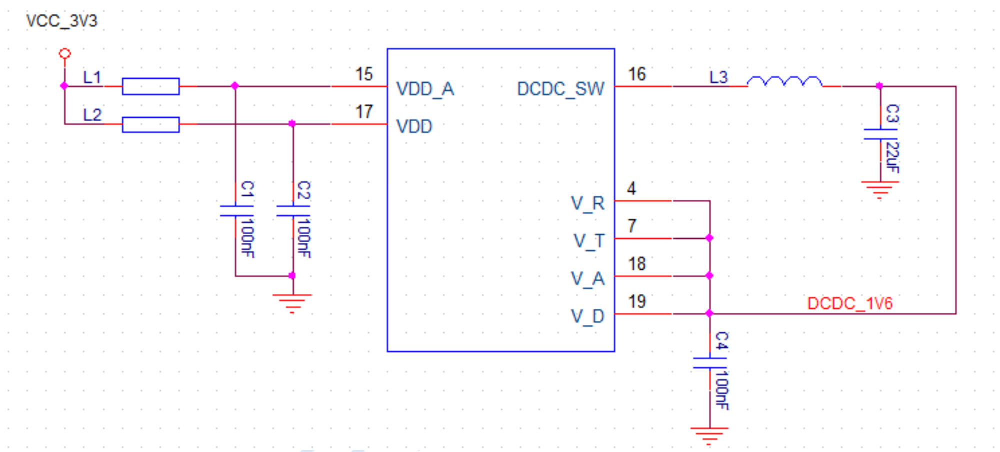

Figure 1-1 Single power supply reference design

1.2 Dual Power Supply

When the chip is powered by both 3.3 V and 1.6 V supplies, Pin 16 (DCDC_SW) of the chip is left floating, while other power pins are connected normally, as illustrated in Figure 1-2.

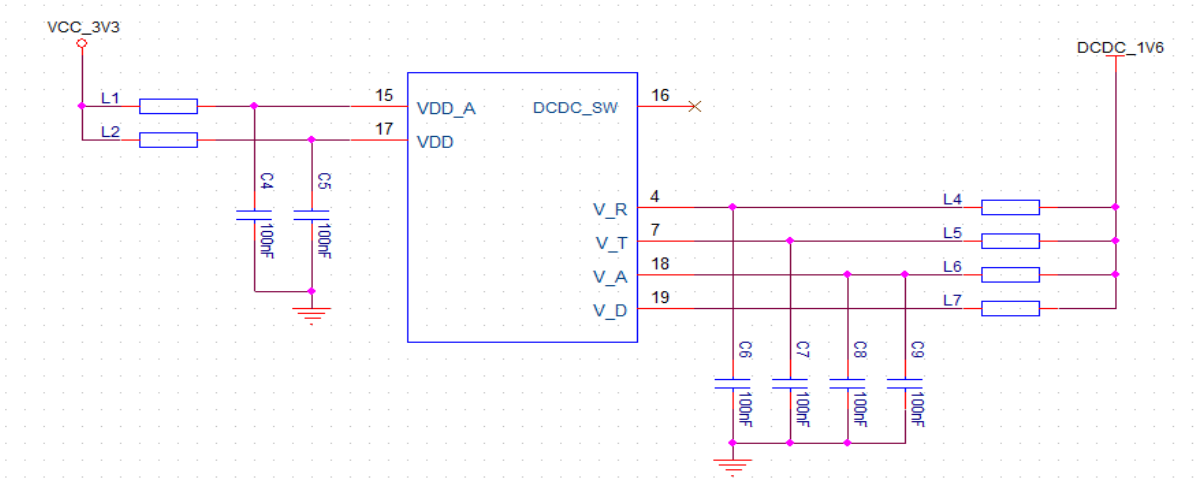

Figure 1-2 Dual power supply reference design

1.3 Component Selection Reference

The component selection for the devices in Figure 1-1 and Figure 1-2 can be referenced in Table 1-1.

Table 1-1 Component Selection Reference

No.	Symbol	Component	Type	Supplier
1	L1~L2, L4~L7	Ferrite bead (31 Ω, ±25%, 100 MHz)	GZ1005D310TF	Sunlord
2	L3	Power inductor (22 μH, ±20%)	SWPA252012S220MT	Sunlord
3	C1~C2, C4~C9	Capacitor (100 nF, ±10%)	CL05B104KO5NNNC	Samsung
4	C3	Capacitor (22 μF, ±10%)	GRM188R61A226ME15L	muRata

2 RF and System Configuration

2.1 Single Chip 1T2R Typical Circuit Design

The typical peripheral circuit design for the S5KM312CL chip with 1 transmitter and 2 receivers is shown in Figure 2-1. It is recommended to configure chip registers using I2C, output data using SPI, and utilize the internal DCDC to supply 1.6 V for the chip.

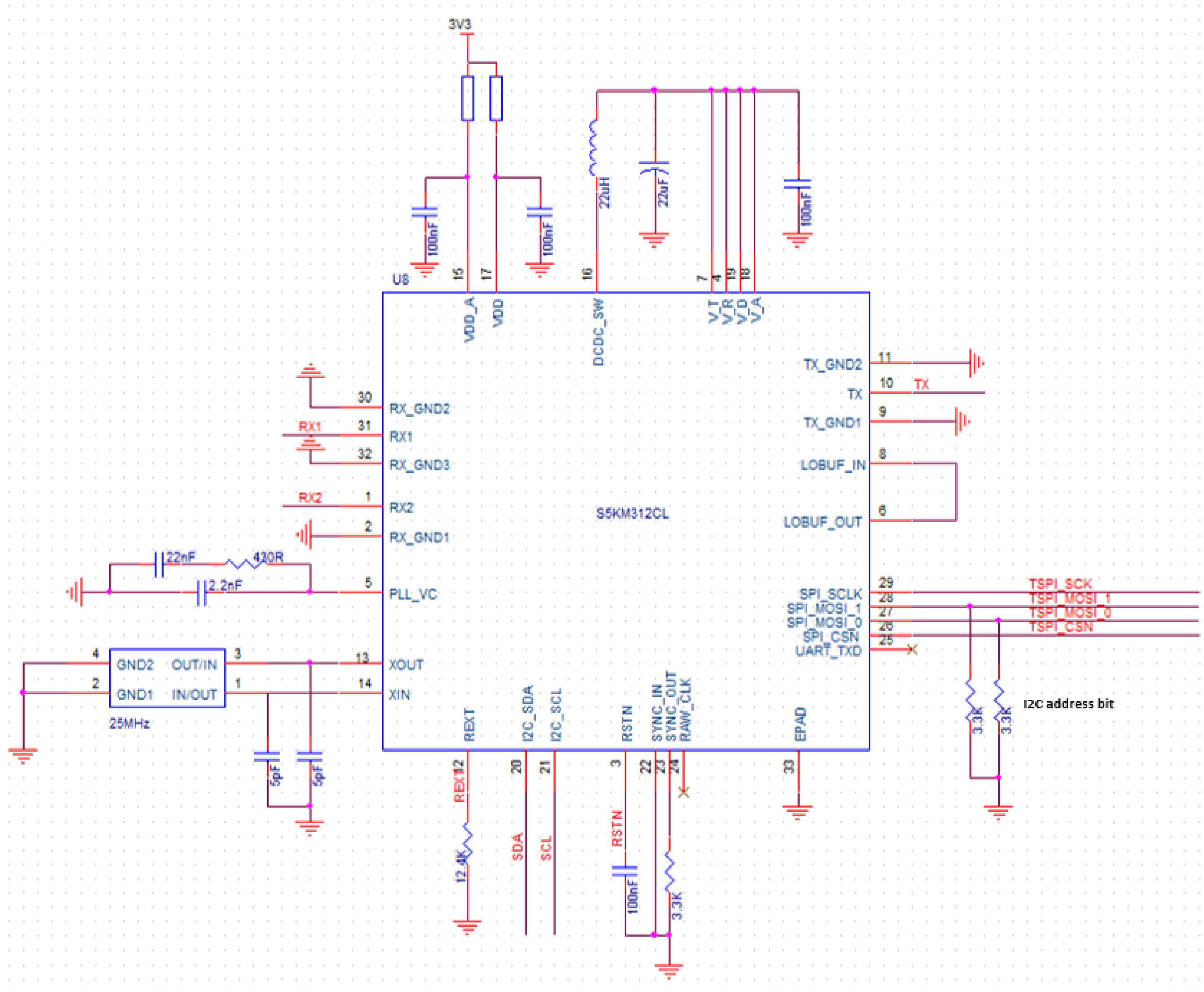

Figure 2-1 Typical circuit reference design for S5KM312CL with 1T2R

2.2 Dual Chip 2T4R Cascade Mode Typical Circuit Design

The typical peripheral circuit design for cascading S5KM312CL chips with 2 transmitters and 4 receivers is illustrated in Figure 2-2. In cascade mode, it is advisable to configure chip registers using I2C, output data using SPI, and utilize the internal DCDC to supply 1.6 V for the chip. If using a dual power supply of 3.3 V and 1.6 V, adjustments corresponding to Figure 1-2 should be made.

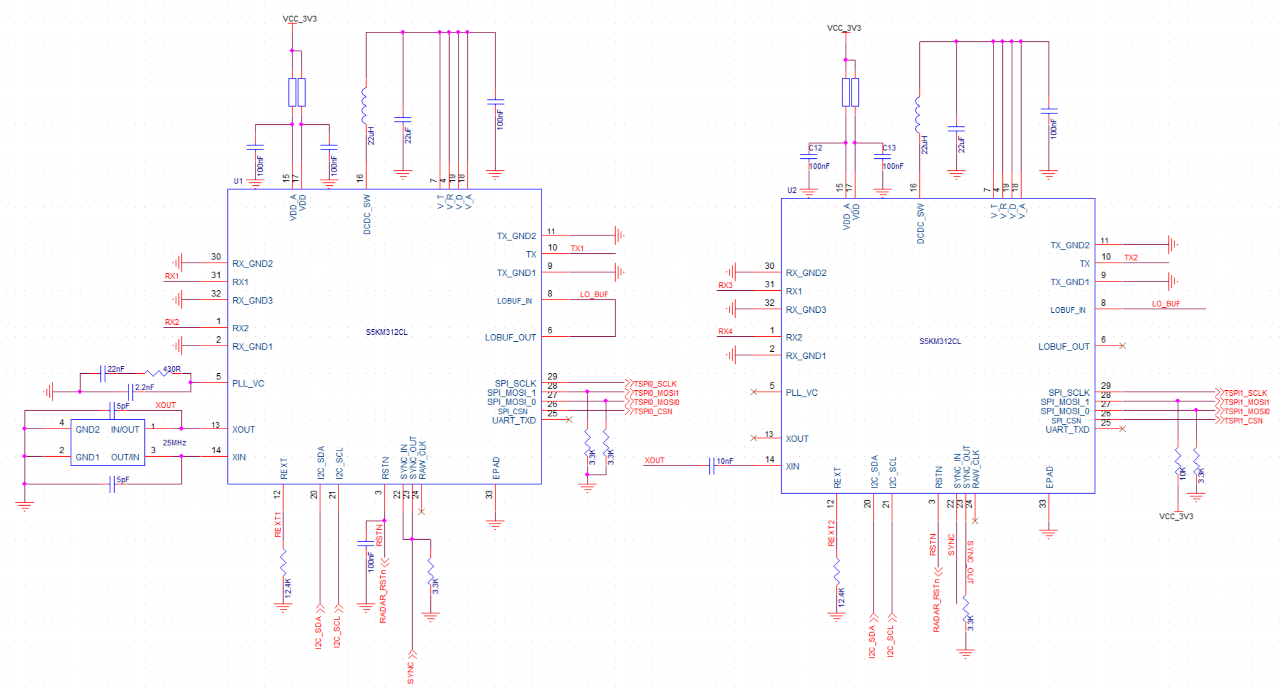

Figure 2-2 Typical circuit reference design for cascaded chips

3 Register Configuration and Data Output Configuration

The configuration modes for the S5KM312CL chip primarily include UART, I2C, and SPI, determined by the logic levels of Pin 23 and Pin 24, as shown in Table 3-1.

Table 3-1 Selection of chip configuration modes

Pin 23	Pin 24	Chip Configuration Mode
Low	Low	UART
Low	High	I2C
High	Low	SPI
High	High	SPI

The data output modes for the S5KM312CL chip mainly consist of GPIO and SPI+UART, determined by the logic level of Pin 25, as indicated in Table 3-2.

Table 3-2 Chip data output modes

Pin 25	Data Output Mode
Low	GPIO (RAW Data)
High	SPI/UART

Note: When Pin 25 is at a high logic level, data can be outputted either solely through SPI or UART, or simultaneously through SPI and UART.

3.1 I2C+(SPI&UART) Mode

It is recommended to configure registers using I2C and output data through SPI & UART within the S5KM312CL chip. Figure 3-1 illustrates a reference circuit for this mode. Pin 24 and Pin 25 can be pulled up by a 10 kΩ resistor or left floating (weak pull-up internally in the chip).

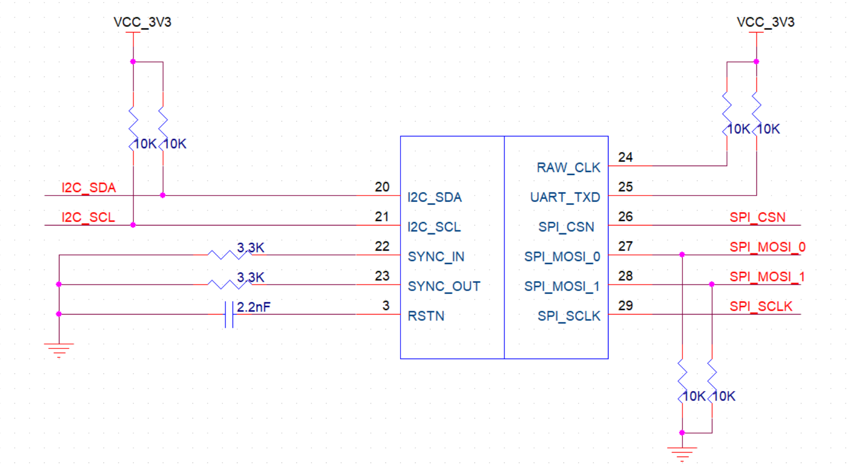

Figure 3-1 Reference circuit for single chip in I2C+(SPI&UART) mode

Figure 3-2 demonstrates a reference circuit for cascaded chip applications of the S5KM312CL chip, utilizing I2C to configure registers and SPI & UART to output data.

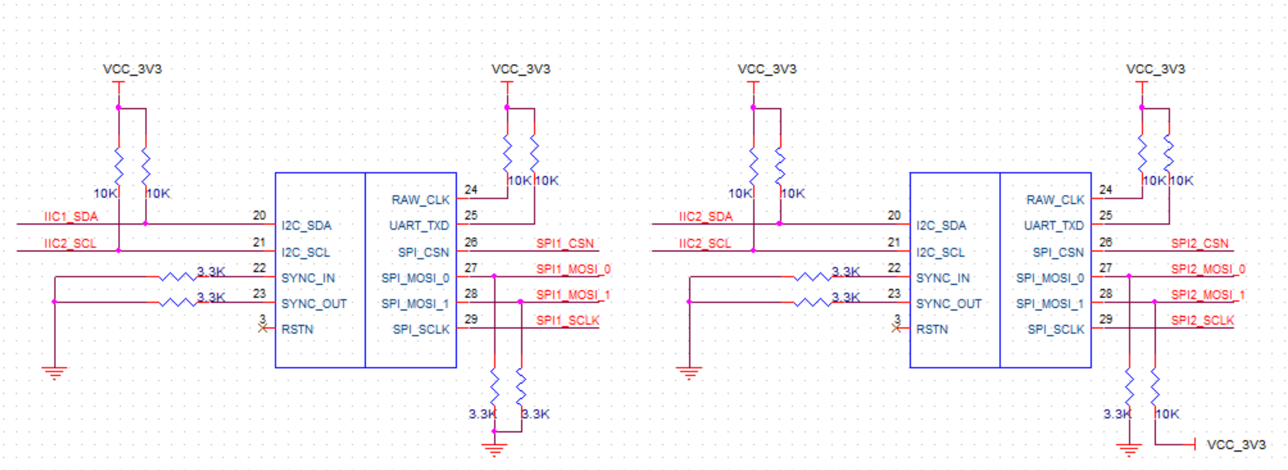

Figure 3-2 Reference circuit for cascaded chips in I2C+(SPI&UART) mode

For inquiries regarding other configuration modes, developers are advised to contact ICL technical support[1].

3.2 I2C Device Address Configuration

The logic levels of Pin 27 and Pin 28 of the S5KM312CL chip determine the I2C device address, as shown in Table 3-3.

Table 3-3 I2C device addresses

Pin 27	Pin 28	I2C Device Address
Low	Low	7'b010_0000
Low	High	7'b010_0001
High	Low	7'b010_0010
High	High	7'b010_0011

[1] For technical support, please send email to: support@iclegend.com.

3.2.1 I2C Device Address for Single Chip Design

When configuring registers using I2C within the S5KM312CL chip for single-chip design, the I2C device address can be set to 0x20. Refer to the circuit in Figure 3-3.

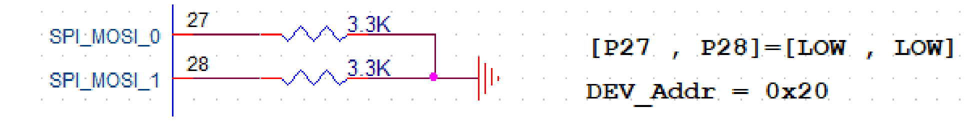

Figure 3-3 Reference circuit for I2C device address in single chip design

3.2.2 I2C Device Address for Chip Cascading

In applications involving cascaded S5KM312CL chips, when configuring registers using I2C, the I2C device address can be set to 0x20 and 0x21. Refer to the circuit in Figure 3-4.

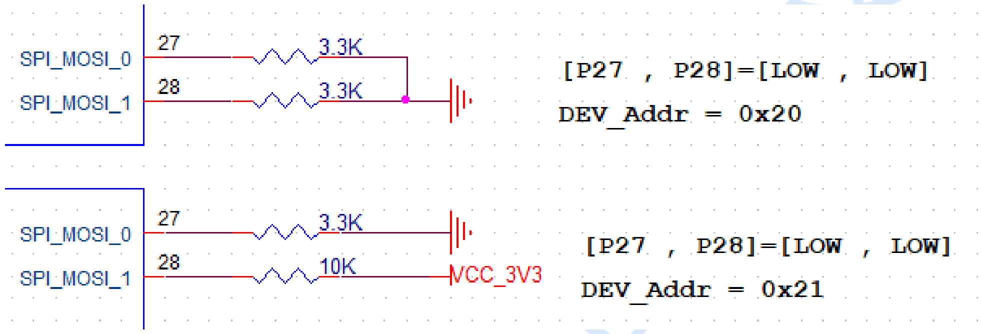

Figure 3-4 Reference circuit for I2C device address in chip cascading

4 Fixed Settings and Crystal Selection

This chapter primarily covers the fixed settings of important pins and crystal selection for the S5KM312CL chip.

4.1 Fixed Settings

4.1.1 SYNC_IN Pin Setting

In single-chip applications of the S5KM312CL chip utilizing I2C for register configuration, Pin 22 remains idle. As this pin is an input pin, it must be grounded to prevent any adverse effects on chip performance due to its unknown state. It is recommended to connect Pin 22 to ground through a series 3.3 kΩ resistor, as shown in Figure 4-1, or it can be directly grounded.

Figure 4-1 Reference circuit for pin 22 in single-chip configuration

In cascaded applications of the S5KM312CL chip, Pin 22 serves as the frame synchronization pin between cascaded chips, as depicted in Figure 4-2.

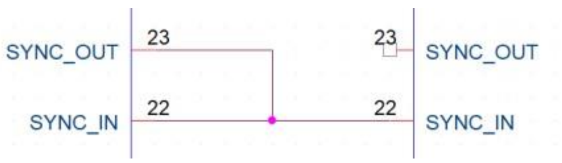

Figure 4-2 Reference circuit for pin 22 in cascaded chip configuration

4.1.2 LOBUF Pin Setting

Pins 6 and 8 of the S5KM312CL chip are used for local oscillator (LO) signal input and output, respectively. In single-chip applications, refer to Figure 4-3 for the circuit configuration.

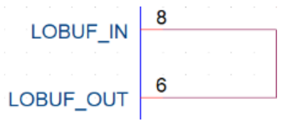

Figure 4-3 Reference circuit for LOBUF pins in single-chip configuration

For cascaded chip applications, refer to Figure 4-4 for the configuration of pin 6 and pin 8.

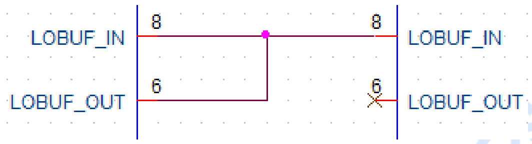

Figure 4-4 Reference circuit for LOBUF pins in cascaded chip configuration

4.1.3 REXT Pin Setting

The REXT pin should be connected to a 12.4 kΩ 1% precision resistor to ground, as shown in Figure 4-5.

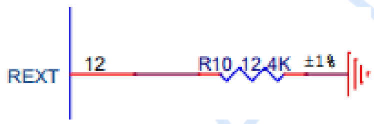

Figure 4-5 Reference circuit for REXT pin

4.1.4 RSTN Pin Setting

The recommended circuit for the RSTN pin is illustrated in Figure 4-6.

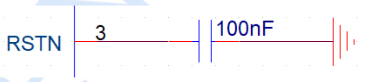

Figure 4-6 Reference circuit for RSTN pin

4.1.5 PLL_VC Pin Setting

The PLL_VC pin is used to set the loop filter bandwidth of the chip's PLL circuit. The recommended circuit, utilizing resistors and capacitors with an accuracy of ±5%, is shown in Figure 4-7.

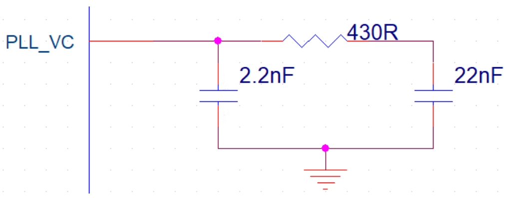

Figure 4-7 Reference circuit for PLL_VC pin

4.2 Crystal Selection

The PLL circuit of the S5KM312CL chip requires a 25 MHz reference crystal oscillator. It is recommended to use a crystal oscillator with a frequency tolerance of less than ±40 ppm under conditions of -40°C to 105°C.

- **Passive Crystal Oscillator (Recommended)**

Refer to Figure 4-8 for the circuit configuration.

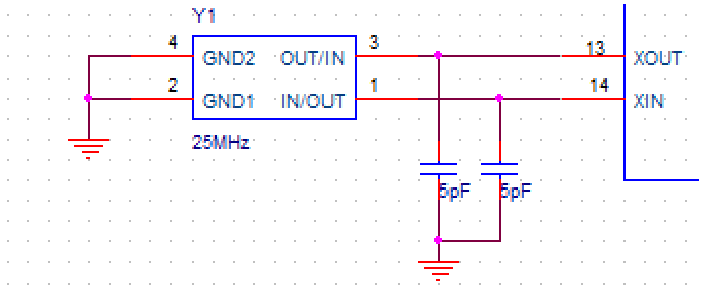

Figure 4-8 Circuit for passive crystal oscillator

Note: The parameters of capacitors are related to the crystal oscillator.

- **Active Crystal Oscillator**

Refer to Figure 4-9 for the circuit configuration.

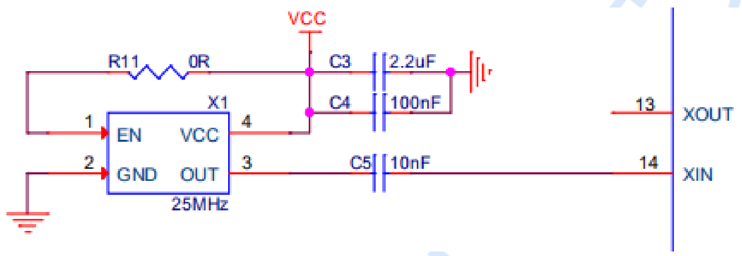

Figure 4-9 Circuit for active crystal oscillator

Notes:

1. See waveform at Xin pin in Figure 4-10.
2. When using an active crystal oscillator, it is recommended to connect a 10 nF AC-coupling capacitor in series with the Xin input pin, as shown by capacitor C5 in Figure 4-9.

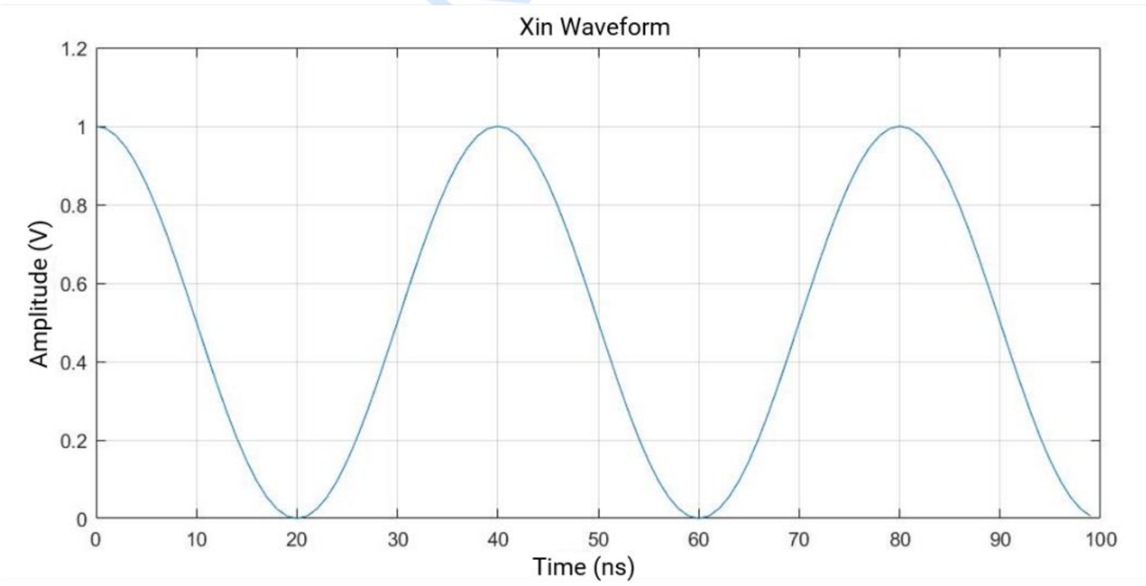

Figure 4-10 Xin waveform of the crystal oscillator

5 PCB Layout

This chapter introduces the PCB layout and layout considerations of the S5KM312CL chip.

5.1 Power Layout

1. POWER 3.3V: Placed close to the 3.3 V pin, with a minimum trace width of 8 mil;
2. POWER 1.6V: Positioned adjacent to the 1.6 V pin, with a minimum trace width of 8 mil;
3. VIA Parameters: Minimum VIA16D8 (pad diameter 16 mil, drill diameter 8 mil);
4. Power supply filtering is crucial, and it is recommended to route POWER, capacitors, and pin traces together.

5.2 PLL_VC Pin

1. The PLL_VC pin is the input for controlling the voltage of the VCO when PLL is locked;
2. The PLL_VC pin is connected to the loop filter circuit, pay attention to placing it near the chip pins during layout (priority over power pins).

5.3 EPAD

1. EPAD: VIA through-holes, dispersed in a 4×4 grid on the EPAD, as shown in Figure 5-1;
2. VIA Parameters: Minimum VIA16D8 (pad diameter 16 mil, drill diameter 8 mil).

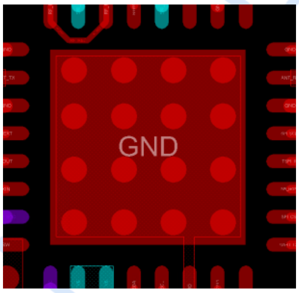

Figure 5-1 EPAD layout reference design

5.4 GND Pins

The treatment of GND pins of the S5KM312CL chip is shown in Figure 5-2, where the content pointed by the blue arrows in the figure is the recommended GND pin reference design.

1. VIA Parameters: VIA16D8 (pad diameter 16 mil, drill diameter 8 mil);
2. TOP chip GND pins are connected to the second layer reference GND of the PCB by VIAs;
3. Chip GND pins should not be directly connected to the same layer EPAD to avoid affecting the isolation between transmission and reception channels.

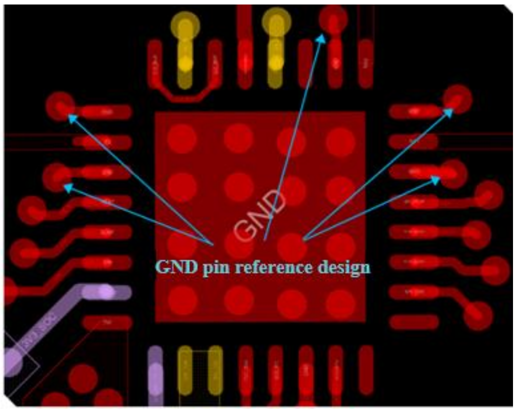

Figure 5-2 GND pin reference design

5.5 LOBUF

As shown in Figure 5-3, the requirements for LOBUF routing are within the blue circle:

1. The trace width is recommended to be 3.5 mil, routed from the bottom of the pin and EPAD;
2. To avoid characteristic impedance mutations and suppress the signal radiation intensity of this pin, it is necessary to ensure the integrity of the reference GND plane around the trace (refer to the gray area), and the area of GND integrity should be as large as possible, subject to simulation results.

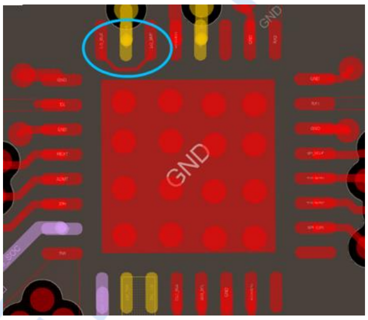

Figure 5-3 LOBUF layout reference design

5.6 Interface Routing

1. The chip configuration buses I2C and SPI, impedance recommended 50 Ω, and require matched length routing;
2. Data output bus SPI, impedance recommended 50 Ω, and require matched length routing, as shown in the blue box in Figure 5-4.

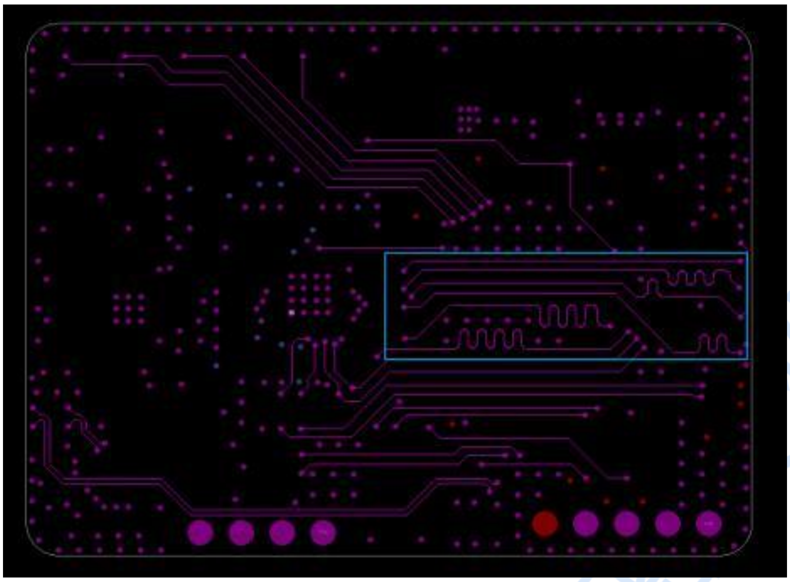

Figure 5-4 Interface routing layout reference design

6 Revision History

Revision	Date	Content
1.2	2024/3/30	Initial release.

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